ABSTRACT OF THE DISCLOSURE

A NAND column has memory cell transistors connected in series by a current passage. Word line drive circuits supply a low voltage to a word lines. A potential supply circuit supplies a high potential higher than the low potential, to a semiconductor region in which the memory cell transistors are formed, to delete contents stored in the memory cell transistors. In deletion verification which verifies that the contents stored in the memory cell transistors have been deleted, a read is executed on each of the word lines. In the read, the word line drive circuit provides the selected one of the word lines with a determination potential used to determine whether or not the contents have been deleted, while providing the other non-selected word lines with a read potential higher than the determination potential.